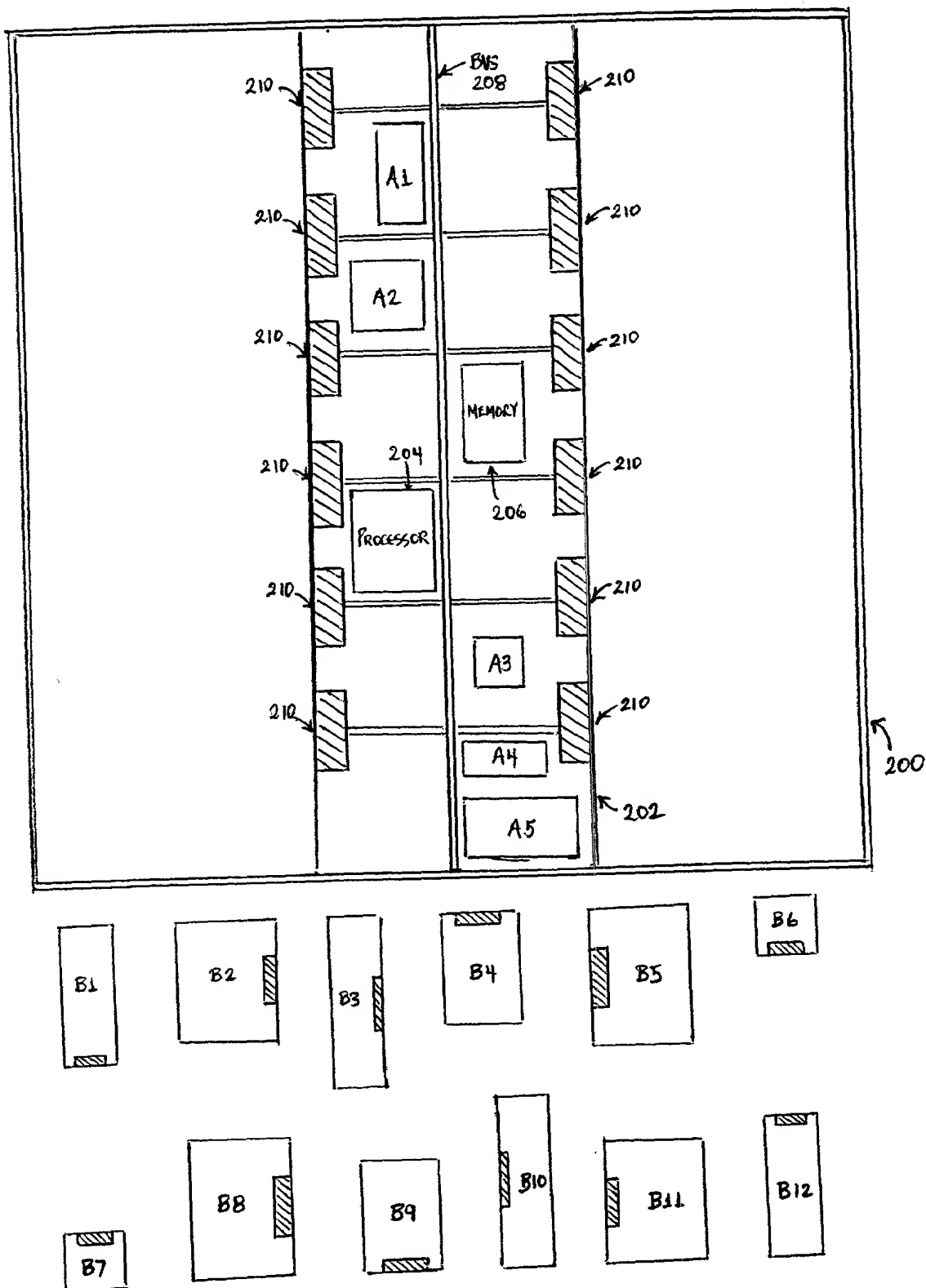


FIGURE 1

 - ANDROGYNOUS
INTERFACE

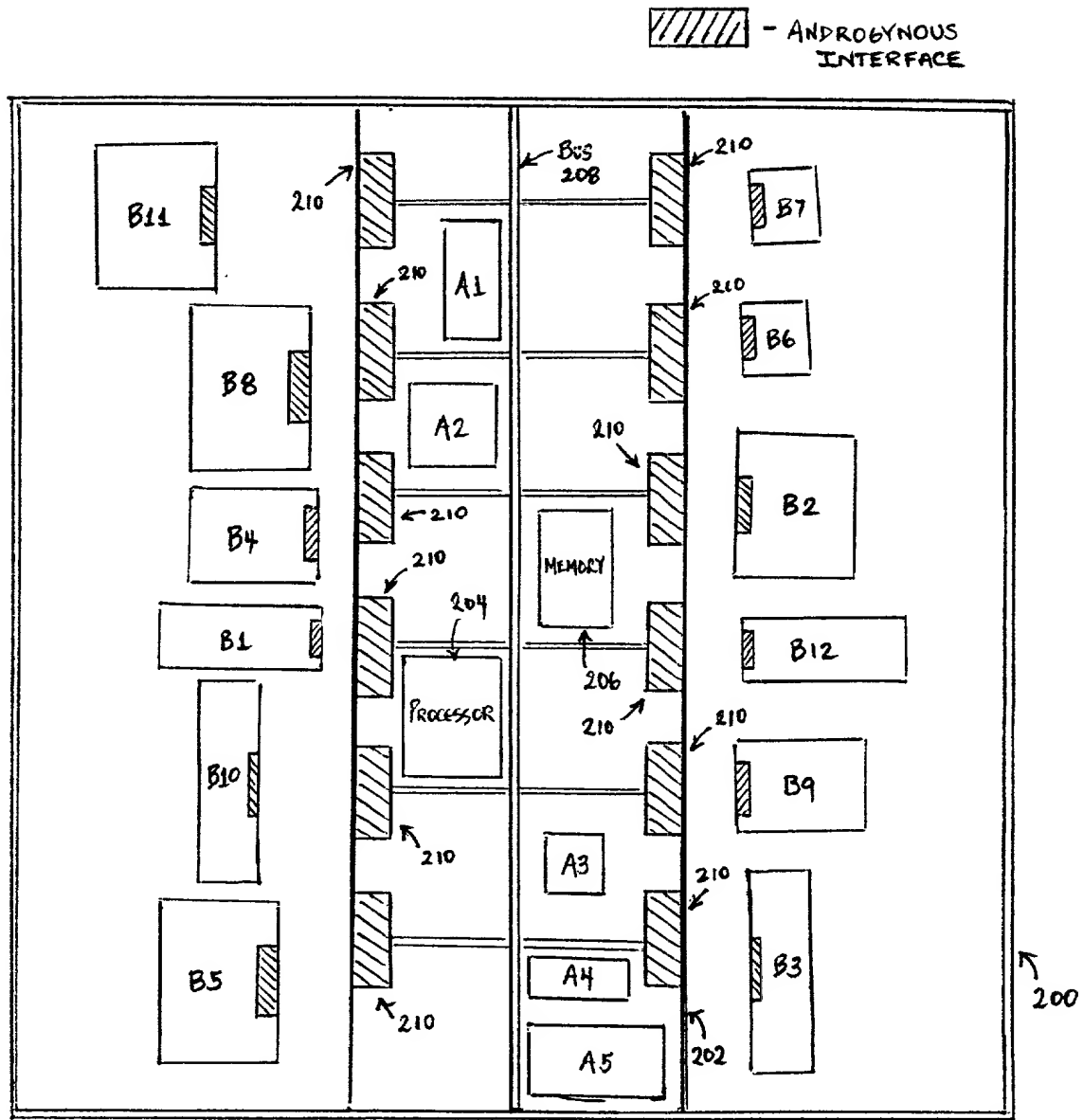


FIGURE 2B

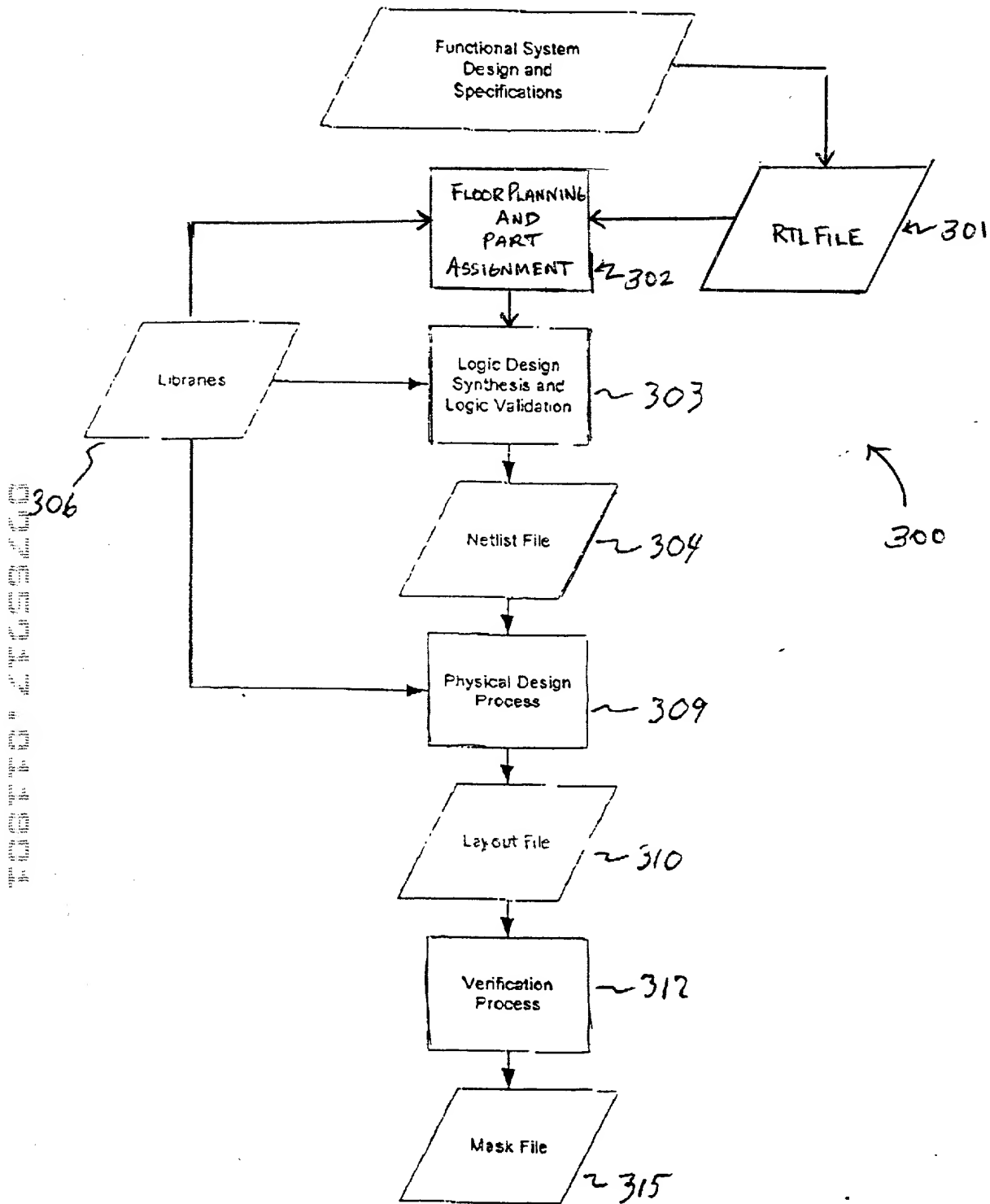


FIGURE 3

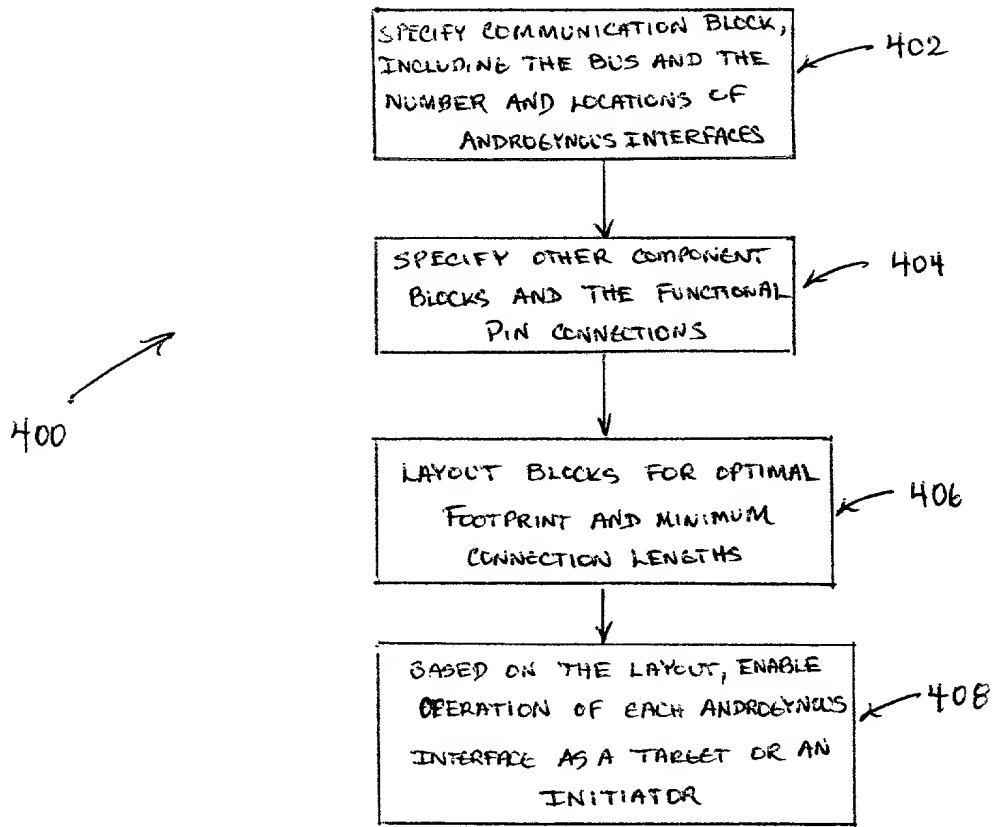


FIG. 4

I/T		T/I
R_data	<-	Data
R_addr	<-	Addr
R_cmd	<-	Cmd
R_Plen	<-	Plen
R_Cfix	<-	Cfix
R_Clen	<-	Clen
R_dval	<-	Dval
Ack	->	R_Ack
R_eop	<-	Eop
R_error	<-	Error
Data	->	R_Data
Addr	->	R_Addr
Cmd	->	R_Cmd
Plen	->	R_Plen
Cfix	->	R_Cfix
Clen	->	R_Clen
Dval	->	R_dval
R_Ack	<-	Ack
Eop	->	R_Eop
Error	->	R_Error

FIG. 5

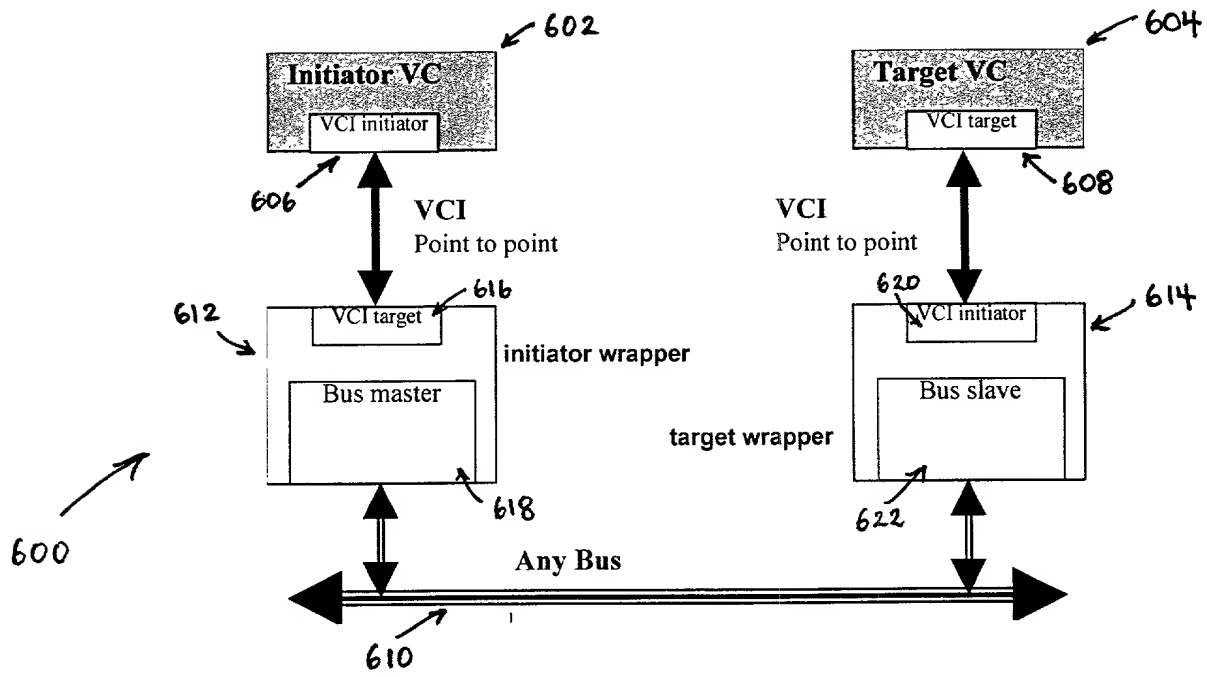


FIG. 6

SOC Master		VCI Slave	VCI Master		SOC Slave
BCLK	==	CLOCK	CLOCK	==	BCLK
BnRES	==	RESETN	RESETN	==	BnRES
r_gnt	<--	CMDACK	CMDACK	<--	gnt
r_req	-->	CMDVAL	CMDVAL	-->	req
r_addr	-->	ADDR[n-1:0]	ADDR[n-1:0]	-->	addr
1111	-->	BE[b-1:0 0:b-1]	BE[b-1:0 0:b-1]	-->	xxxx
0	-->	CFIXED	CFIXED	-->	x
0	-->	CLEN[q-1:0]	CLEN[q-1:0]	-->	x
r_cmd	-->	CMD[1:0]	CMD[1:0]	-->	cmd
1	-->	CONTIG	CONTIG	-->	x
r_data	-->	WDATA[8b-1:0]	WDATA[8b-1:0]	-->	data
r_eop	-->	EOP	EOP	-->	eop
0	-->	CONST	CONST	-->	x
r_d_size	-->	PLEN[k-1:0]	PLEN[k-1:0]	-->	d_size
0	-->	WRAP	WRAP	-->	x
gnt	-->	RSPACK	RSPACK	-->	r_gnt
req	<--	RSPVAL	RSPVAL	<--	r_req
data	<--	RDATA [8b-1:0]	RDATA [8b-1:0]	<--	r_data
eop	<--	REOP	REOP	<--	r_eop
error	<--	RERROR	RERROR	<--	r_error

FIG. 7

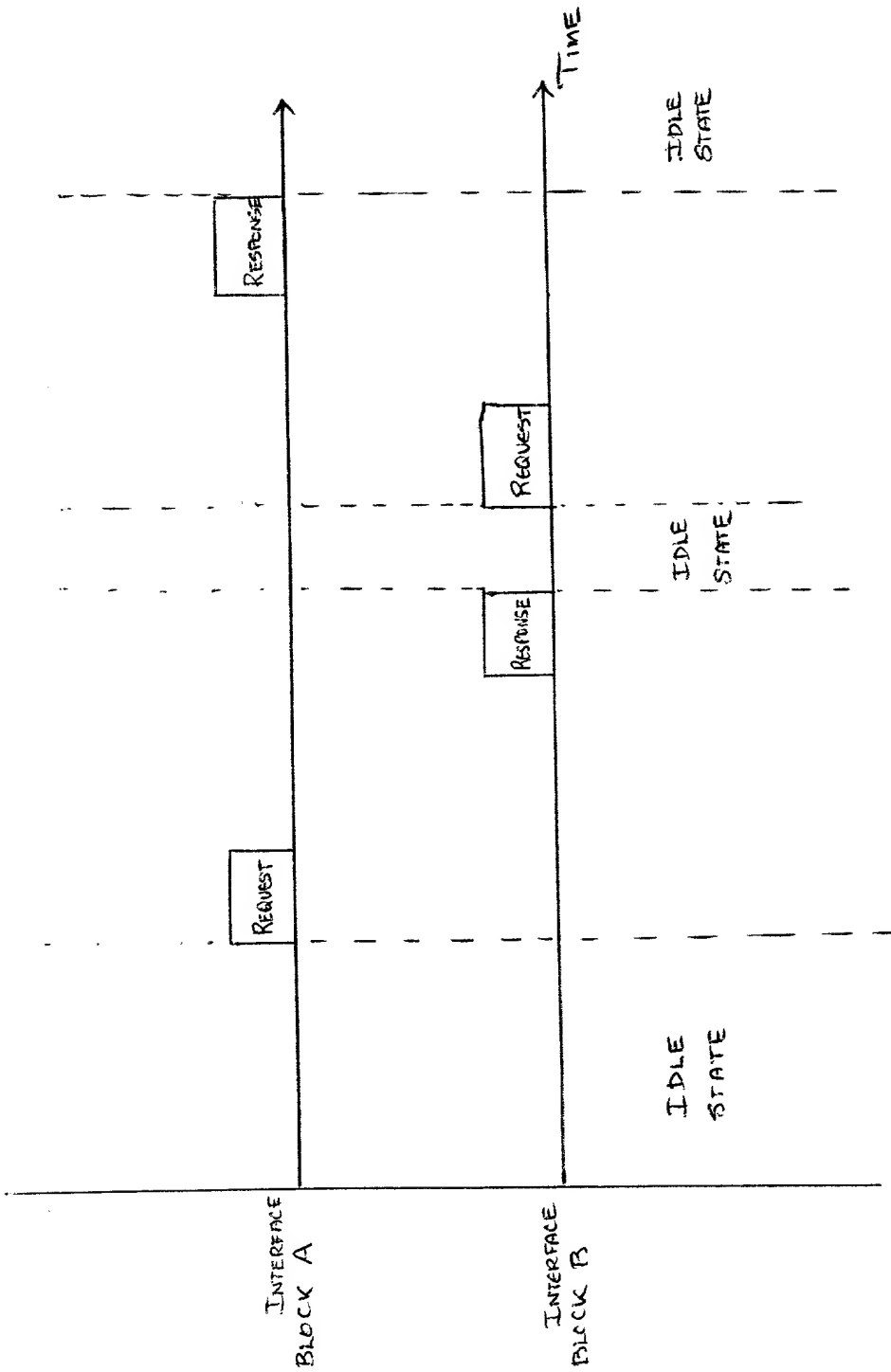


FIG. 8